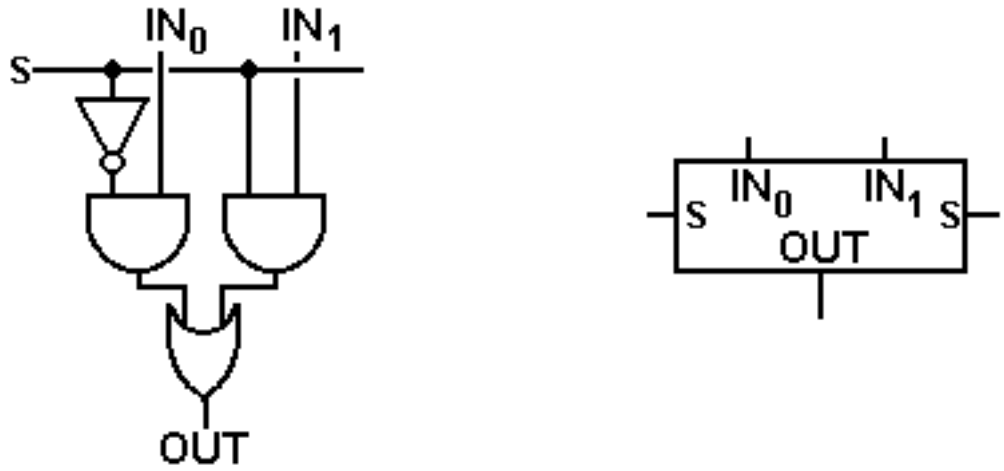
8/24/12

Selector

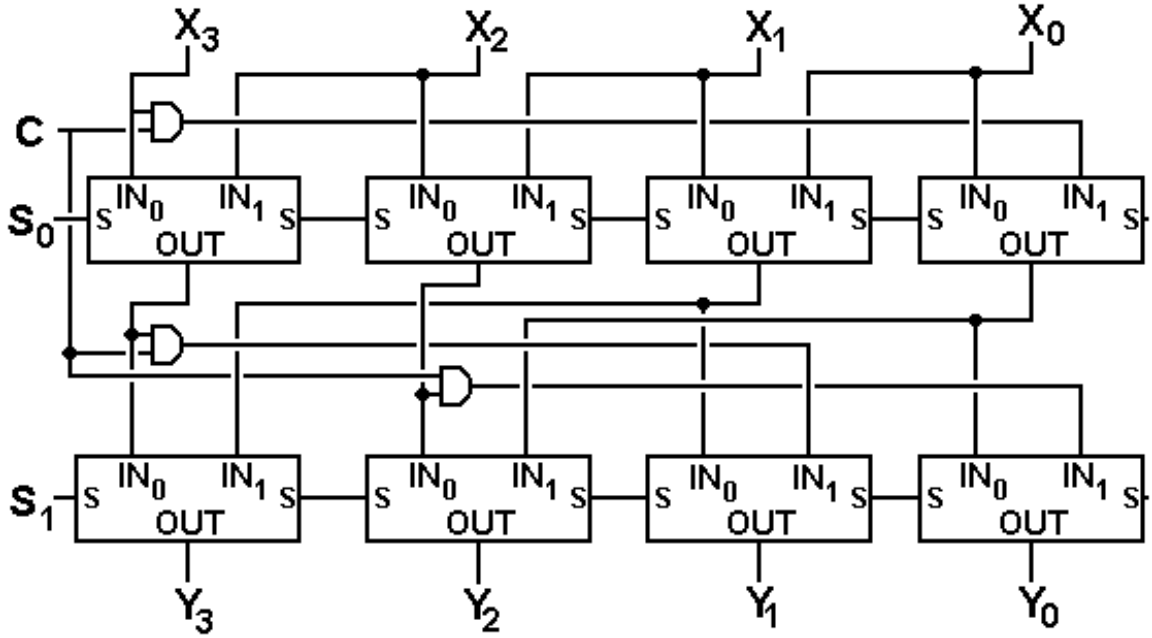
Image of a selector:



Reference: http://www.edwardbosworth.com/My5155Text_V07_HTM/MyText5155_Ch06_V07.htm

Barrel shifter

Image of 4 bit barrel shifter where C = 1:



Reference: http://www.edwardbosworth.com/My5155Text_V07_HTM/MyText5155_Ch06_V07.htm

4 bit barrel shifter has 4x inputs and 2s inputs (s inputs to specify how many bits to shift)

Example of a right cyclic shift: 101011 -> 110101

Barrel shifter is hardware logic to implement cyclic shift

Used also in computer architecture

Priority Scheduler

- First 1 in inputs from left is the only 1 value outputted
- Input: 0011 -> Output: 0010
- Useful for requests and only letting one input to access resource at a time
- If all inputs are 0 all outputs are 0

$o_1 = i_1$
$o_2 = \bar{i}_1 * i_2$
…
$o_k = \bar{i}_1 * \bar{i}_2 * \ldots * \bar{i}_{k-1} * i_k$

Area is important because of chip size. Goal is to optimize area and delay and to find the optimum tradeoff between the two.

$\bar{i}_1, \bar{i}_2, \bar{i}_3, \ldots \bar{i}_n$ Given these inputs n is a power of 2
$\{\bar{i}_1 \bar{i}_2\}, \{\bar{i}_3 \bar{i}_4\}, \{\bar{i}_5 \bar{i}_6\}, \{\bar{i}_7 \bar{i}_8\}$ 2 in a block, need n/2 gates
$\{\bar{i}_1 \bar{i}_2 \bar{i}_3 \bar{i}_4\}, \{\bar{i}_5 \bar{i}_6 \bar{i}_7 \bar{i}_8\}$ 4 in a block, need n/4 gates
…
Area: O(n), Delay: log(n)

$O_{12} = \bar{i}_1 * \bar{i}_2 * \bar{i}_3 * \ldots * \bar{i}_{11} * i_{12}$

At most n = 11 = At most log(n) bits $(1011)_2$

$(\bar{i}_1, \bar{i}_2, \ldots \bar{i}_8)$ $(\bar{i}_9, \bar{i}_{10})$ $(\bar{i}_{11})$

Area: $n * \log(\log(n))$
Delay: $\log(n) + \log(\log(n)) = \log(n * \log(n)$